CLAIM AMENDMENTS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) An electronic circuit comprising:

first and second pipeline stages;~~-and~~

a first latch positioned between the first and second pipeline stages; and

a first latch control circuit connected to the first latch, said latch control circuit receiving a first control signal, said first control signal being randomly-generated and indicating a mode of operation of the electronic circuit;

wherein the electronic circuit is adapted to operate in a normal mode in which the first latch is opened and closed in response to an enable signal controlled by the first latch control circuit, and a reduced mode in which the first latch is held open by the first latch control circuit~~ to reduce a current peak associated with the opening and closing of the latch~~.

2. (Canceled)

3. (Currently Amended) ~~An~~ The electronic circuit~~ as claimed in~~ of claim 1, the electronic circuit further comprising:

a third pipeline stage and a second latch, the second latch positioned between the second and third pipeline stages.

4. (Currently Amended) ~~An~~ The electronic circuit ~~as claimed in~~ of claim 3, wherein, when the electronic circuit is operating in the reduced mode, ~~both of~~ the first and second latches are held open ~~to reduce the current peaks associated with the opening and closing of the latches~~.

5. (Currently Amended) ~~An~~ The electronic circuit ~~as claimed in~~ of claim 3, wherein, when the electronic circuit is operating in the reduced mode, one of the first and the second latches is held open ~~to reduce the current peak associated with the opening and closing of that latch~~.

6. (Currently Amended) ~~An~~ The electronic circuit ~~as claimed in~~ of claim 5, wherein the one of the first and the second latches held open changes over time.

7. (Currently Amended) ~~An~~ The electronic circuit ~~as claimed in~~ of claim 6, wherein the first and second latches are held open for different lengths of time.

8. (Currently Amended) ~~An~~ The electronic circuit ~~as claimed in~~ of claim 1, wherein ~~the length of time that~~ the electronic circuit operates in the reduced mode for varying time periods~~varies~~.

9. (Currently Amended) ~~An~~ The electronic circuit ~~as claimed in~~ of claim 3, further comprising:

a second latch control circuit connected to the second latch, said second latch control circuit receiving a second control signal, said second control signal being randomly-generated and indicating the mode of operation of the electronic circuit.

10. (Canceled)

11. (Currently Amended) ~~An~~ The electronic circuit ~~as claimed in claim 10~~ of claim 9, wherein the first and second control signals ~~indicates~~ indicate whether the first latch, the second latch, or both latches are to be held open when the electronic circuit is operating in the reduced mode.

12. (Canceled)

13. (Currently Amended) A method of operating an electronic circuit, the electronic circuit comprising first and second pipeline stages and a first latch positioned between the first and second pipeline stages, the method comprising:

operating the electronic circuit in a normal mode in which the first latch is opened and closed in response to an enable signal, and a reduced mode in which the first latch is held open in response to a first control signal, said first control signal being randomly-generated and indicating whether the first latch is to be held open

when the electronic circuit is operating in the reduced mode ~~to reduce a current peak associated with the opening and closing of the latch~~.

14. (Currently Amended) ~~A~~ The method ~~as claimed in~~ of claim 13, the electronic circuit further comprising a third pipeline stage and a second latch, the second latch positioned between the second and third pipeline stages, ~~stages;~~ the method further comprising:

holding the second latch open when the electronic circuit is operating in the reduced mode in response to a second control signal, said second control signal being randomly-generated and indicating whether the second latch is to be held open when the electronic circuit is operating in the reduced mode ~~to reduce a current peak associated with the opening and closing of the second latch~~.

15. (Currently Amended) ~~A~~ The method ~~as claimed in~~ of claim 14, wherein the first latch and the second latch are held open at different times when the electronic circuit is operating in the reduced mode.

16. (Currently Amended) ~~A~~ The method ~~as claimed in~~ of claim 15 wherein the first latch and the second latch are held open for different lengths of time.

17. (Currently Amended) ~~A~~ The method ~~as claimed in~~ of claim 14, wherein, when the electronic circuit is operating in the reduced mode, both the first latch and the second latch are held open.

18. (Currently Amended) ~~A~~ The method ~~as claimed in~~ of claim 13, wherein ~~the length of time that~~ the electronic circuit operates in the reduced mode ~~varies~~ for varying time periods.